Amendments to the Claims:

Please add new claims 7-16, and please amend claims 1 and 5 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (currently amended) An internal voltage generation circuit, comprising:

a voltage divider for dividing a level of an internal voltage to provide a divided internal voltage;

a comparator connected to an external voltage and the internal voltage, for comparing the divided internal voltage with a reference voltage to generate a compared output; and

a driver connected to the external voltage for supplying the external voltage to the internal voltage in response to the compared output of the comparator, wherein when the external voltage is reduced to a level that is lower than the internal voltage, the compared output inactivates the driver, and the driver prevents the supplying of the reduced external voltage to the internal voltage and the internal voltage maintains a constant level.

2. (original) The internal voltage generation circuit of claim 1, wherein the voltage divider comprises resistors serially connected between the internal voltage and ground voltage.

3. (original) The internal voltage generation circuit of claim 1, wherein the internal voltage generation circuit further comprises a reference voltage generator for generating the reference voltage having a predetermined voltage level by dividing a level of the external voltage.

4. (original) The internal voltage generation circuit of claim 1, wherein the comparator comprises:

a first diode-type NMOS transistor the source of which is connected to the external

voltage;

a second diode-type NMOS transistor the source of which is connected to the internal voltage;

a first PMOS transistor the source and bulk of which are connected to drains of the first and second NMOS transistors, and the gate and drain of which are connected to each other;

a second PMOS transistor the source and bulk of which are connected to the drains of the first and second NMOS transistors, and the gate of which is connected to a gate of the first PMOS transistor;

third and fourth NMOS transistors connected to drains of the first and second PMOS transistors and gated to the reference voltage and the divided internal voltage, respectively; and

a fifth NMOS transistor connected between drains of the third and fourth transistors and ground voltage and gated to a signal enabling the comparator.

5. (currently amended) The internal voltage generation circuit of claim 4, wherein the driver is a PMOS transistor the source of which is connected to the external voltage, the gate of which is connected to the output of the comparator, the drain of which is connected to the internal voltage, and where the drains of the first and second NMOS transistors of the comparator are connected to a back bias voltage <u>of the PMOS transistor of the driver</u>.

6. (original) The internal voltage generation circuit of claim 4, wherein the first and second NMOS transistors are native transistors the threshold voltages of which are 0V.

7. (new) The internal voltage generation circuit of claim 4, wherein the compared output of the comparator is provided at the drain of the second PMOS transistor.

8. (new) An internal voltage generation circuit, comprising:

a voltage divider for dividing a level of an internal voltage to provide a divided internal voltage;

a comparator connected to an external voltage and the internal voltage, for comparing the divided internal voltage with a reference voltage to generate a compared output; and

a driver connected to the external voltage for supplying the external voltage to the internal voltage in response to the compared output of the comparator, wherein the driver comprises a transistor having a back-bias voltage connected to an internal node of the comparator.

9. (new) The internal voltage generation circuit of claim 8, wherein the voltage divider comprises resistors serially connected between the internal voltage and ground voltage.

10. (new) The internal voltage generation circuit of claim 8, wherein the internal voltage generation circuit further comprises a reference voltage generator for generating the reference voltage having a predetermined voltage level by dividing a level of the external voltage.

11. (new) The internal voltage generation circuit of claim 8, wherein the comparator comprises:

a first diode-type NMOS transistor the source of which is connected to the external voltage;

a second diode-type NMOS transistor the source of which is connected to the internal voltage;

a first PMOS transistor the source and bulk of which are connected to drains of the first and second NMOS transistors at the internal node, and the gate and drain of which are connected to each other;

a second PMOS transistor the source and bulk of which are connected to the drains of the first and second NMOS transistors at the internal node, and the gate of which is connected to a gate of the first PMOS transistor;

third and fourth NMOS transistors connected to drains of the first and second PMOS transistors and gated to the reference voltage and the divided internal voltage, respectively; and

a fifth NMOS transistor connected between drains of the third and fourth transistors and ground voltage and gated to a signal enabling the comparator.

12. (new) The internal voltage generation circuit of claim 11, wherein the driver is a PMOS transistor the source of which is connected to the external voltage, the gate of which is connected to the output of the comparator, the drain of which is connected to the internal voltage, and where the drains of the first and second NMOS transistors of the comparator are connected to a back bias voltage of the transistor of the driver.

13. (new) The internal voltage generation circuit of claim 11, wherein the first and second NMOS transistors are native transistors the threshold voltages of which are 0V.

14. (new) The internal voltage generation circuit of claim 11, wherein the compared output is provided at the drain of the second PMOS transistor.

15. (new) The internal voltage generation circuit of claim 8, wherein the internal node comprises a common node of the comparator between a first terminal of a first transistor configured as a diode-type transistor, a second terminal of the first transistor being connected to the external voltage, and a first terminal of a second transistor configured as a diode-type transistor, a second terminal of the second transistor being connected to the internal voltage.

16. (new) The internal voltage generation circuit of claim 15, wherein the first transistor comprises an NMOS transistor having a gate and source of which are coupled to the external voltage, and having a drain of which is coupled to the common node, and wherein the second transistor comprises an NMOS transistor having a gate and source of which are coupled to the internal voltage, and having a drain of which is coupled to the common node.